Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	915	parameter$5 same map$4 same rule	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/29 08:21
L2	224	(parameter$5 same map$4 same rule) and match$4 and document	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/29 08:22
L3	4	(parameter$5 same map$4 same rule) and match$4 and document and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/29 08:24
L4	1	(parameter$5 same map$4 same rule) and match$4 and document and DRC	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/29 08:26
L5	18	(parameter$5 same map$4) and match$4 and document and DRC	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/29 08:28
L6	105	(parameter$5 same (DRC or (design adj rule adj checker))) and match$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/29 08:30
L7	40	(parameter$5 same (DRC or (design adj rule adj checker))) and match$4 and "716"/$.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/29 08:43
L8	9	(parameter$5 same (DRC or (design adj rule adj checker))) and match$4 and table and "716"/$. ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/04/29 08:43

	Document ID	Title	Current OR
1	US 20050076316 A1	Design-manufacturing interface via a unified model	716/4
2	US 20050010890 A1	Design-based monitoring	716/19
3	US 20040243949 A1	Parameter checking method for on-chip ESD protection circuit physical design layout verification	716/4
4	US 20040191650 A1	Phase shift masking for complex patterns with proximity adjustments	430/5
5	US 20040168139 A1	Identifying line width errors in integrated circuit designs	716/5
6	US 20040163069 A1	Integrated circuit schematics and layouts	716/11
7	US 20040163064 A1	Line width check in layout database	716/5
8	US 20040163063 A1	Line width check in layout database	716/5
9	US 20040163062 A1	Checking layout accuracy in integrated circuit designs	716/5
10	US 20040163061 A1	Design rule checking integrated circuits	716/5
11	US 20040163060 A1	Line width error check	716/5
12	US 20040139408 A1	Split and merge design flow concept for fast turnaround time	716/5
13	US 20040098689 A1	Rapid chip management system	716/11
14	US 20040025126 A1	System and method for providing compliant mapping between chip bond locations and package bond locations for an integrated circuit	716/5
15	US 20040015797 A1	Line width check in layout database	716/5
16	US 20030229866 A1	Method for improving chip yields in the presence of via flaring	716/5

	Document ID	Title	Current OR
17	US 20030229860 A1	Method, system and computer product to produce a computer-generated integrated circuit design	716/1
18	US 20030061583 A1	Shape and look-up table based design rule checking (DRC) for physical verification of integrated circuit layouts	716/5
19	US 20020197543 A1	Phase conflict resolution for photolithographic masks	430/5
20	US 20020192575 A1	Method for designing and making photolithographic reticle, reticle, and photolithographic process	430/5
21	US 20020160280 A1	Method and layout for high density reticle	430/5
22	US 6862723 B1	Methodology of generating antenna effect models for library/IP in VLSI physical design	716/13
23	US 6859915 B1	Signal line impedance verification tool	716/5
24	US 6845492 B1	Signal via impedance adjustment tool	716/2
25	US 6839887 B1	Method and system for predictive multi-component circuit layout generation with reduced design cycle	716/11
26	US 6775806 B2	Method, system and computer product to produce a computer-generated integrated circuit design	716/1
27	US 6769103 B2	Line width check in layout database	716/5
28	US 6733929 B2	Phase shift masking for complex patterns with proximity adjustments	430/5
29	US 6606735 B1	Method and system for using error and filter layers in each DRC rule	716/5
30	US 6519756 B1	Method and apparatus for building an integrated circuit	716/18

	Document ID	Title	Current OR
31	US 6480995 B1	Algorithm and methodology for the polygonalization of sparse circuit schematics	716/11
32	US 6457164 B1	Hetergeneous method for determining module placement in FPGAs	716/8
33	US 6389558 B1	Embedded logic analyzer for a programmable logic device	714/39
34	US 6374395 B1	Methodology for generating a design rule check notch-error free core cell library layout	716/11
35	US 6324673 B1	Method and apparatus for edge-endpoint-based VLSI design rule checking	716/11
36	US 6305000 B1	Placement of conductive stripes in electronic circuits to satisfy metal density requirements	716/5
37	US 6298319 B1	Incremental compilation of electronic design for work group	703/26
38	US 6275971 B1	Methods and apparatus for design rule checking	716/5
39	US 6238824 B1	Method for designing and making photolithographic reticle, reticle, and photolithographic process	430/5
40	US 6182247 B1	Embedded logic analyzer for a programmable logic device	714/39